

CLAIMS

- 1 1. A method for programming a memory cell comprising a first electrode, a second
2 electrode and an inter-electrode layer of material, comprising:
3 applying stress to the inter-electrode layer to induce a progressive change in a
4 property of said inter-electrode layer.
- 1 2. The method of claim 1, wherein said inter-electrode layer comprises a dielectric,
2 and said property is resistance.
- 1 3. The method of claim 1, wherein said inter-electrode layer comprises an ultra-thin
2 layer.
- 1 4. The method of claim 1, wherein said inter-electrode layer of material comprises
2 silicon dioxide having a thickness less than 20 Angstroms.
- 1 5. The method of claim 1, wherein said inter-electrode layer of material comprises
2 silicon oxynitride having a thickness less than 20 Angstroms.
- 1 6. The method of claim 1, wherein said inter-electrode layer of material comprises
2 silicon dioxide having a thickness less than 15 Angstroms.
- 1 7. The method of claim 1, wherein said inter-electrode layer of material comprises
2 silicon oxynitride having a thickness less than 15 Angstroms.
- 1 8. The method of claim 1, wherein said material in said inter-electrode layer of
2 material comprises at least one of Al_2O_3 , YTa_2O_5 , HfO_2 , Y_2O_3 , CeO_2 , TiO_2 , HfSi_xO_y ,
3 HfSiON , HfAlO_x , TaO_xN_y , ZrO_2 , ZrSi_xO_y , La_2O_3 , and ZrO_2 .

1 9. The method of claim 1, including, after applying said stress to cause said
2 progressive change in the property, generating a signal indicating the property, and
3 comparing the signal with a reference signal to verify programming of desired data.

1 10. The method of claim 1, including, after applying said stress to cause said
2 progressive change in the property, generating a signal indicating the property, and
3 comparing the signal with a reference signal to verify programming of desired data; and
4 if said verifying fails, then applying stress again to cause additional change in said
5 property.

1 11. The method of claim 1, wherein said memory cell comprises an element of a
2 memory array, and a plurality of levels of said property are associated with respective
3 numbers of program cycles applied to the memory array, and including:
4 maintaining a record of a number of program cycles applied to the memory array;
5 producing a reference signal corresponding with said number of program cycles;
6 after applying said stress to cause said progressive change in the property,
7 generating a signal indicating the property, and comparing the signal with said reference
8 signal to verify programming of desired data.

1 12. The method of claim 1, wherein said memory cell comprises an element of a
2 memory array, and a plurality of levels of said property are associated with respective
3 numbers of program cycles applied to the memory array, and including:
4 maintaining a record of a number of program cycles applied to the memory array;
5 providing a source of two reference signals corresponding with first and second
6 program cycles;
7 after applying said stress to cause said progressive change in the property,
8 generating a signal indicating the property, and comparing the signal with a reference
9 signal corresponding with said number of program cycles selected from said two
10 reference signals to verify programming of desired data.

1 13. The method of claim 1, wherein said memory cell comprises an element of a
2 memory array, and a plurality of levels of said property are associated with respective
3 numbers of program cycles applied to the memory array, and including:
4 maintaining a record of a number of program cycles applied to the memory array;
5 providing a source of three reference signals corresponding with first, second, and
6 third program cycles;
7 after applying said stress to cause said progressive change in the property,
8 generating a signal indicating the property, and comparing the signal with a reference
9 signal corresponding with said number of program cycles selected from said three
10 reference signals to verify programming of desired data.

1 14. The method of claim 1, wherein said memory cell comprises an element of a
2 memory array, and a plurality of levels of said property are associated with respective
3 numbers of program cycles applied to the memory array, and including:
4 maintaining a record of a number of program cycles applied to the memory array;
5 providing a source of a plurality of reference currents corresponding with
6 respective numbers of program cycles;
7 after applying said stress to cause said progressive change in the property,
8 generating a signal current indicating the property, and comparing the signal current with
9 a selected reference current selected from said plurality of reference currents and
10 corresponding with said number of program cycles, to verify programming of desired
11 data.

1 15. The method of claim 1, wherein a plurality of levels of said property are
2 associated with respective values of multiple bits of data in the memory cell, and
3 including:
4 providing a value for said multiple bits of data to be programmed in the memory
5 cell;
6 producing a reference signal corresponding with said value;

after applying said stress to cause said progressive change in the property,
generating a signal indicating the property, and comparing the signal with said reference
signal to verify programming of said value.

16. The method of claim 1, wherein a plurality of levels of said property are
associated with respective values of multiple bits of data in the memory cell, and
including:

providing a value for said multiple bits of data to be programmed in the memory
cell;

providing a source of a plurality of reference currents corresponding with
respective values for said multiple bits;

after applying said stress to cause said progressive change in the property,
generating a signal current indicating the property, and comparing the signal current with
a selected reference current selected from said plurality of reference currents and
corresponding with said value, to verify programming of said value.

17. The method of claim 1, wherein a plurality of levels of said property are
associated with respective values of multiple bits of data in the memory cell, and
including:

providing a value for said multiple bits of data to be programmed in the memory
cell;

providing a source of three reference currents corresponding with respective
values for two bits;

after applying said stress to cause said progressive change in the property,
generating a signal current indicating the property, and comparing the signal current with
a selected reference current selected from said three reference currents and corresponding
with said value, to verify programming of said value.

18. The method of claim 1, wherein a plurality of levels of said property are
associated with respective values of multiple bits of data in the memory cell, and
including:

4 providing a value for said multiple bits of data to be programmed in the memory
5 cell;
6 providing a source of seven reference currents corresponding with respective
7 values for three bits;
8 after applying said stress to cause said progressive change in the property,
9 generating a signal current indicating the property, and comparing the signal current with
10 a selected reference current selected from said seven reference currents and
11 corresponding with said value, to verify programming of said value.

1 19. The method of claim 1, wherein after applying said stress, sensing whether said
2 property exceeds a first reference level to indicate a first stored value, and then applying
3 stress another time to cause additional progressive change in said property to change the
4 stored value, and sensing whether said property exceeds a second reference level to
5 indicate the changed stored value.

1 20. The method of claim 1, wherein said applying stress includes:
2 applying a first program pulse to the cell having a first pulse height and a first
3 pulse width;
4 determining whether the cell is programmed in response to the first program
5 pulse; and if not
6 applying a program retry pulse to the cell;
7 determining whether the cell is programmed in response to the program retry
8 pulse; and if not
9 iteratively applying another program retry pulse to the cell and determining
10 whether the cell is programmed, until the cell is determined to be programmed or a
11 maximum number of retries is made;
12 wherein the program retry pulses have respective pulse widths and pulse heights
13 which vary according to a pattern in which at least one program retry pulse has a different
14 pulse width or different pulse height than other program retry pulses in the pattern.

- 1 21. A method for programming a memory array multiple times, comprising:
2 applying stress to selected memory cells in said array to set values of a property
3 of said selected memory cells;
4 maintaining a record of a number of program cycles applied to said array;
5 producing a reference signal corresponding with said number of program cycles,
6 wherein said reference signal is changed progressively for succeeding program cycles;
7 after applying said stress, generating a signal indicating the value of said property
8 programmed in a selected memory cell, and comparing the signal with said reference
9 signal to sense data stored in the selected memory cell.
- 1 22. The method of claim 21, wherein said providing a reference signal includes:
2 providing a source of two reference signals corresponding with first and second
3 program cycles, and selecting one of the two reference signals for the first program cycle
4 and selecting the other of the two reference signals for the second program cycle.
- 1 23. The method of claim 21, wherein said providing a reference signal includes:
2 providing a source of first and second sets of reference signals, said first and
3 second sets corresponding with respective first and second program cycles, and said first
4 and second sets comprising respective pluralities of reference signals corresponding with
5 respective values for multiple bits of data stored in the selected memory cell;
6 selecting a reference signal from the first set for the first program cycle and
7 selecting a reference signal from the second set for the second program cycle.
- 1 24. The method of claim 21, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer has a property
4 characterized by a progressive change in said property in response to said stress.
- 1 25. The method of claim 21, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second

3 electrode and an inter-electrode layer, and said inter-electrode layer comprises an ultra-
4 thin layer.

1 26. The method of claim 21, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of
4 silicon dioxide less than 20 Angstroms thick.

1 27. The method of claim 21, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of
4 silicon dioxide less than 15 Angstroms thick.

1 28. The method of claim 21, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of
4 silicon oxynitride less than 20 Angstroms thick.

1 29. The method of claim 21, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of
4 silicon oxynitride less than 15 Angstroms thick.

1 30. A method for resetting data stored in a memory array, where data in the memory
2 array is stored by setting a property of memory cells in the array above or below a
3 reference level to indicate a data value, comprising:
4 changing the reference level.

1 31. The method of claim 30, wherein said changing the reference level resets data
2 stored in the array without changing said property in memory cells in the array.

1 32. The method of claim 30, wherein said changing the reference level comprises
2 changing a reference used for sensing a level of said property of memory cells in the
3 array.

1 33. The method of claim 30, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said property comprises resistance, and
4 wherein said changing the reference level comprises changing a reference current used
5 for sensing a level of resistance of memory cells in the array.

1 34. The method of claim 30, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer is characterized by a
4 progressive change in said property in response to said stress.

1 35. The method of claim 30, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer comprises an ultra-
4 thin layer.

1 36. The method of claim 30, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of
4 silicon dioxide less than 20 Angstroms thick.

1 37. The method of claim 30, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of
4 silicon dioxide less than 15 Angstroms thick.

1 38. The method of claim 30, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of
4 silicon oxynitride less than 20 Angstroms thick.

1 39. The method of claim 30, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of
4 silicon oxynitride less than 15 Angstroms thick.

1 40. A method for programming data stored in a memory array multiple times,
2 comprising:
3 setting a property of memory cells in the array above or below a first reference
4 level to indicate data values in said memory cells;
5 resetting the array by changing the reference level to a second reference level; and
6 setting the property of memory cells in the array above or below the second
7 reference level to indicate said data values in said memory cells.

1 41. The method of claim 40, wherein said changing the reference level comprises
2 changing a reference used for sensing a level of said property of memory cells in the
3 array.

1 42. The method of claim 40, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer is characterized by a
4 progressive change in said property in response to said stress.

1 43. The method of claim 40, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said property comprises resistance, and

4 wherein said changing the reference level comprises changing a reference current used
5 for sensing a level of resistance of memory cells in the array.

1 44. The method of claim 40, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer comprises an ultra-
4 thin layer.

1 45. The method of claim 40, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of
4 silicon dioxide less than 20 Angstroms thick.

1 46. The method of claim 40, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of
4 silicon dioxide less than 15 Angstroms thick.

1 47. The method of claim 40, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of
4 silicon oxynitride less than 20 Angstroms thick.

1 48. The method of claim 40, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of
4 silicon oxynitride less than 15 Angstroms thick.

1 49. A method for programming multiple bits of data in memory cells in a memory
2 array multiple times, comprising:

3 setting a property of memory cells in the array above or below a first set of
4 reference levels to indicate multiple bits of data in said memory cells;
5 resetting the array by changing the first set of reference levels to a second set of
6 reference levels; and
7 setting the property of memory cells in the array above or below the second set of
8 reference levels to indicate said multiple bits of data in said memory cells.

1 50. The method of claim 49, wherein said changing the first set of reference levels to
2 the second set of reference levels comprises changing references used for sensing levels
3 of said property of memory cells in the array.

1 51. The method of claim 49, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said property comprises resistance, and
4 wherein said changing the first set of reference levels to the second set of reference levels
5 comprises changing reference currents used for sensing levels of resistance of memory
6 cells in the array.

1 52. The method of claim 49, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer is characterized by a
4 progressive change in said property in response to said stress.

1 53. The method of claim 49, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer comprises an ultra-
4 thin layer.

1 54. The method of claim 49, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second

3 electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of
4 silicon dioxide less than 20 Angstroms thick.

1 55. The method of claim 49, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of
4 silicon dioxide less than 15 Angstroms thick.

1 56. The method of claim 49, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of
4 silicon oxynitride less than 20 Angstroms thick.

1 57. The method of claim 49, wherein said memory array comprises an array of
2 memory cells, and said memory cells respectively comprise a first electrode, a second
3 electrode and an inter-electrode layer, and said inter-electrode layer comprises a layer of
4 silicon oxynitride less than 15 Angstroms thick.